DIGITAL MAGNETIC RECORDING/REPRODUCING APPARATUS

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of application
Serial No. 09/185,097 filed on November 3, 1998, the
5    contents of which are incorporated herein by reference in
their entirety.


BACKGROUND OF THE INVENTION

The present invention relates to digital magnetic
recording/reproducing apparatuses such as magnetic disk
10   recorders, and particularly to a signal processing system
and apparatus for recording digital data at high density.

The demand for high-density recording and fast
processing in magnetic disk recorders has more and more
escalated.  The signal processing techniques in the
15   signal recording and reproducing system to support these
requirements have also been developed towards
high-density recording and fast processing.  As to the
recording code, the coding rate R has been increased, and
now the main coding rate R in current use is R=8/9.  In
20   addition, recently a higher rate recording code of
R=16/17 has started to be practically used.  Moreover, a
partial response equalization system is employed in order
to prevent the signal-to-noise ratio from being reduced
by the increase of the intercode interference involved
25   with the high-density recording.  PR4ML (Partial Response

Class 4 with Maximum Likelihood Detection) is utilized to detect a signal sequence nearest to the reproduced signal by the Viterbi algorithm (best likelihood sequence estimation) using a known interference occurring in the reproducing channel. A device for this purpose is already incorporated as an LSI (Large Scale Integrated Circuit) in a magnetic disk product. It is known that if the input signal sequence to the PR4ML processor is binary data of 0, 1, the minimum squared Euclidean distance (MSED) between signal sequences produced by PR4ML is 2. Therefore, PR4ML is improved 3 dB in its tolerance to noise over the peak detection system (MSED=1) for deciding magnetic information by only 0, 1 without the best likelihood sequence estimation.

In order to achieve higher-density recording than PR4ML, it is necessary to use such a signal processing technique as to increase the MSED. For this purpose, there are EPR4ML (Extended PR4ML), and EEPR4ML (Extended EPR4ML). These are the extensions of the PR4ML idea. The values of MSED for those extensions are known to be 4, 6 (binary conversion), respectively. In addition, the channel state number is 8 for EPR4ML, and 16 for EEPR4ML.

Fig. 2 is a block diagram of a conventional digital magnetic recording/reproducing apparatus. As illustrated, on the recording side, an information sequence of "0"s and "1"s as digital data is converted into a high rate code such as R=8/9 or 16/17 by a

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recording coder 201. The recording code, as well known, has a limited number of successive "0"s provided to prevent the timing extraction and gain control (not shown in Fig. 2) in the reproducing section from being reduced

5    in their performances. The recording coded sequence is further supplied to a precoder 202, thereby being converted into a code in which 1/(1+D) is treated as a transfer function. Only when data of "1" is supplied to the precoder 202, the output is changed from just the

10   preceding value. Here, D is the delay operator, and the delay time is equal to the bit distance. The precoder 202 is able to suppress the decoded error propagation length after the Viterbi detection on the reproducing section to a limited value. The precoded sequence is

15   supplied through an amplifier 203 to a record head 204, by which it is recorded on a magnetic recording medium 205 as magnetic information.

On the reproducing side, the magnetic information recorded on the magnetic recording medium 205 is

20   reproduced by a reproduce head 206, and supplied to an amplifier 207, thereby being converted into an analog electric signal. This signal is supplied to an A/D converter 208, which samples it at each bit interval, thereby converting it into a digital signal. The digital

25   signal is fed to a PR equalization circuit 209, which then equalizes it into partial response channels such as PR4, EPR4, and EEPR4. The PR equalization can be easily

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realized by a well known transversal filter.  The output
from the PR equalization circuit 209 contains noise added
up to a signal level determined by the PR channel
characteristic.  Here, the noise contains the medium

5    noise, the noise mixed from the reproduce-side head, and
the noise caused by A/D quantization.  These noises, when
passed through the PR equalization circuit 209, become
colored noises with a correlation.  The equalized signal
with the noise added is supplied to a Viterbi detector

10   210 that performs MLSE (Maximum Likelihood Sequence
Estimation).  Thus, it produces the most probable data
sequence, or a data sequence most likely to resemble the
input signal sequence.  Since the reverse characteristic
(1+D) to the precoder 202 can be produced as NRZI (Non

15   Return to Zero Inverted) within the Viterbi detector as
well known, a postcoder can be removed.  The data
sequence from the Viterbi detector 210 is decoded into
the information sequence by a recording decoder 211.

        Thus, this conventional digital magnetic

20   recording/reproducing apparatus employs a high-rate
recording code, and combines the partial response and
Viterbi detection, thereby increasing the signal-to-noise
ratio of the reproduced signal for high-density
recording.

25      In recent years, other various signal processing
systems for higher-density recording have been discussed
in addition to the above-described conventional

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apparatus.  As a powerful one of those systems, there is
a list Viterbi algorithm (hereinafter referred to as an
LVA).  In this system, the Viterbi detector 210 detects
the most reliable data sequence (best sequence), the
5    second most reliable data sequence (2nd best sequence),
the third most reliable data sequence (3rd best
sequence), ... , and the nth most reliable data sequence
(nth best sequence), produces these as proposed
sequences, or candidates, detects a decoding error of
10   each candidate by use of CRC (Cyclic Redundancy Check) or
the like, and generates a decoded output of candidates
with no decoding error.  The LVA is able to greatly
improve the decoding error characteristic of the Viterbi
detector.  The details of the LVA are described in N.
15   Seshadri et al., "List Viterbi Decoding Algorithms with
Applications", IEEE Transactions on Communications, Vol.
42, No. 2/3/4, February/March/April 1994, pp. 313-323.
The LVA was originally contrived for application to a
communications field such as mobile radio communication,
20   but it has not yet been applied to a magnetic
recording/reproducing apparatus.  The present invention
fundamentally applies the LVA to a magnetic
recording/reproducing apparatus as will be described
later with respect to various embodiments.  However, a
25   simple application of the conventional idea directly to
the apparatus cannot achieve high-density recording.
This will be described in detail later.

The basic idea of the LVA will be described using as an example an EPR4 channel with reference to the trellis diagram of Fig. 3. Fig. 3 shows the structure of the EPR4 channel with respect to time (here, time 0 to 8).

5      The number of channel states is 8. The states 000, ... , 111 are expressed as 0, ... , 7, respectively. When -1 and +1 (which correspond to binary data 0, 1, respectively) are applied to the respective states, the associated PR equalization signals (expressed in binary conversion

10     values as illustrated) are produced, making the channel states transitional.

It is now assumed that the state at time 0 is 1. When data 1 is applied at time 1, the PR equalization output of 2 is produced, and thus the channel state is

15     shifted from 1 to 3.

The equalization signal of an EPR4 channel takes five values of 2, 1, 0, -1, and -2. In Fig. 3, it is assumed that the line A indicates the state transition sequence (path) corresponding to the correct data

20     sequence. However, as a result of the Viterbi detection, the decoded signal may sometimes be in error as indicated by line B. As will be seen from the figure, the squared Euclidean distance is 4 between the correct decoded path (the equalization signal value sequence is 0, 0, 0, 1, 1,

25     -1, 0, 1) and the erroneous decoded path (the equalization signal value sequence is 0, 0, 1, 2, 1, -1, -1, 0). This is an error event of MSED=4. In general,

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the decoding error characteristic of the maximum likelihood sequence estimation is determined by MSED. The error event of MSED=4 occurs at the highest frequency in EPR4ML.

On the other hand, the LVA estimates and produces a plurality of candidates (2nd best, 3rd best, … , nth best sequences) including the maximum likelihood estimated sequence (best sequence) in the order of higher probability (likelihood ratio). If there are two candidates, the path (correct sequence) indicated by the line A is produced as the best sequence, and the path (error sequence) indicated by the line B is produced as the 2nd best sequence as shown in Fig. 3. Since these candidates include the correct decoded path, the correct one can be selected by CRC error detection to both sequences. Therefore, the LVA can remove the error event of MSED=4, and a larger Euclidean distance error event will occur. In other words, the MSED is equivalently expanded, and thus the decoded error characteristic can be improved. In the case of EPR4ML, the MSED is expanded to 6 (an example of the error event of MSED=6 is indicated by line C). This means that the S/N (signal-to-noise ratio) of the reproduced signal is improved about 1.8 dB. Although an EPR4 channel has here been given as an example, the LVA can be applied to other PR channels than an EPR4 channel, and hence the decoded error characteristics can be improved.

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The LVA is classified into a serial system and a
parallel system as described in the above-given document.
The serial system, at the time of the Viterbi detection,
decides the 2nd best sequence if the best sequence

5   becomes erroneous as the candidate, the 3rd best sequence
if the 2nd best sequence is erroneous, and similarly the
nth best sequence if the (n-1)th best sequence is
erroneous.  Thus, the LVA repeats the sequence estimation
processing until there is no error.  Of course, since n

10  is practically definite, when error is still present
after n repetitions, a signal indicating the presence of
decoding error is transmitted to the transmission side,
requesting retransmission.

The parallel system, at the time of Viterbi

15  detection, produces n candidates at a time, and selects
one with no error decided by CRC.  In this case, too,
when error is detected in all candidates, the signal
indicating the presence of decoding error is transmitted
to the transmission side, requesting retransmission.

20  When the LVA is applied to a magnetic
recording/reproducing apparatus, the serial system is
able to achieve LVA detection by a relatively simple
construction, but has too large a maximum processing
delay (n times as large as in the prior art) to be

25  applied to fast processing.  The parallel system needs a
large amount of ACS (Add, Compare, Select) operations (n
times as much as in the prior art) for estimating a

proposed candidate, but can perform fast processing since candidates can be produced in parallel. Therefore, the parallel system capable of fast processing is suited to the magnetic recording. The increase of the circuit scale causes practically no important problem since the process for LSIs (Large Scale Integrated Circuits) has recently fast developed.

According to the above document, the LVA of the parallel system periodically fixes both of the starting and ending states to one (in the other cases than these states, N states) on the trellis diagram as shown in Fig. 4. On the starting side, the likelihood ratios of all candidates are reinitialized to the same value as the likelihood ratio of the best sequence. This is because the LVA needs to select n candidates having different likelihood ratios to be estimated within an interval of M bits, that is, to always choose n different candidates of unlike likelihood ratios within this interval. Therefore, the n candidates to be detected at intervals of M bits each are all sure to be different.

In this system, if the path memory length necessary for LVA detection is represented by K bits and the block length of a CRC code by L bits, then the relation of $K \geq L$ must be satisfied, that is, the necessary path memory length is required to be set longer than or equal to the CRC block length. The reason for this will be explained with reference to Fig. 5. Fig. 5 shows the

relations between the LVA path memory length and the CRC block length. The number of candidates is 2. Here, it is assumed that the S/N ratio is so high as to consider a probability that two or more error events will occur to

5  be negligibly small. When the path memory length is larger than the CRC block length, the 2nd best sequence covers, even if an error event occurs in the first block of the best sequence, that error as shown in Fig. 5 at (a), that is, a correct sequence is included in the first

10  or second block of either the best or 2nd best sequence. However, when the path memory length is smaller than the CRC block length, errors can arise in both sequences over a CRC block length as shown in Fig. 5 at (b). This phenomenon in the prior art is caused because a different

15  sequence is always selected for the LVA at each path memory length. Thus, the LVA must be matched to the CRC block length, and the necessary path memory length must be set to be longer than or equal to the CRC block length.

20  When the LVA is applied to a magnetic recording/reproducing apparatus, the following problem is caused.

(1) Since the necessary path memory length for the LVA detector is required to be larger than the CRC block

25  length, making the CRC block length long (more than about 100 bits) makes it impractical to construct the LVA detector. In the conventional system, the LVA is

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utilized in a communications field such as mobile radio communication, and thus it is not necessary to extremely increase the coding rate. Therefore, the CRC block length is as short as at most 10 bits (the path memory

5  length is about 20 bits), and the coding rate may be about 8/10. In practice, however, since the conventional system employs a combination of a convolution code of rate 1/2 as a code for constructing the trellis diagram in addition to the CRC code, the coding rate of the whole

10  system is substantially as fairly low as 4/10. For the magnetic recording, the coding rate of the whole system is required to be more than 8/9 for high-density recording. Thus, the CRC block length for this purpose becomes very long (more than about 100 bits), and thus

15  the LVA detector that needs a path memory length longer than that cannot be practically constructed since the processing delay becomes remarkably large.

    (2) In the conventional system, each of the starting and ending state sides is periodically fixed to one state

20  on the trellis diagram, and the likelihood ratios of all candidates on the starting state side are initialized to be the likelihood ratio of the best sequence. Thus, different candidates are always obtained at each path memory length. Therefore, the number of codes that can

25  be assigned on the trellis is considerably limited, and thus the possible recording code rate is low (about 1/2)

on the trellis.  In other words, the conventional LVA
cannot achieve more than the current rate 8/9.

        Under the presence of the above problems, the
conventional LVA cannot accomplish high-density
recording.


SUMMARY OF THE INVENTION
        In view of the above problems, it is an object of
the invention to provide a digital magnetic
recording/reproducing apparatus capable of maintaining
the coding rate as high as more than 8/9, and performing
higher-density recording than in the prior art.
        In order to solve the problems, according to the
invention, the LVA detector has means provided which
detects data sequences up to (2n-1)th (n > 1) in the
order of higher likelihood ratio, and which produces n
candidates when the contents of the (i-1)th path memory
coincide with those of the ith path memory (i=2, 3, ... ,
n) and the absolute value of the difference between the
(i-1)th and (2i-1)th likelihood ratios is smaller than a
decision threshold by replacing the likelihood ratio and
the path memory for the ith best candidate by those for
the (2i-i)th best candidate.
        In addition, another means is provided which
initializes the likelihood ratio of the ith best
candidate to be the likelihood ratio of the (i-1)th best
candidate with a constant difference value added thereto

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when the contents of the (i-1)th path memory and the ith
path memory (i=2, 3, … , n) of the n candidates are equal
to each other.

BRIEF DESCRIPTION OF THE DRAWINGS

5      Fig. 1 is a block diagram of a digital magnetic
recording/reproducing apparatus according to the
invention.

       Fig. 2 is a block diagram of a conventional digital
magnetic recording/reproducing apparatus.

10      Fig. 3 is a trellis diagram of an EPR4 channel.

       Fig. 4 is a trellis diagram of a parallel LVA in the
prior art.

       Fig. 5 is a diagram useful for explaining the
problem caused by the relation between the LVA path

15  memory length and the CRC block length.

       Fig. 6 is a block diagram of the construction of an
ACS circuit of the LVA detector according to the first
embodiment of the invention.

       Fig. 7 is a block diagram of the construction of a

20  path memory circuit of the LVA detector according to the
first embodiment of the invention.

       Fig. 8 is a block diagram of an ACS circuit of the
LVA detector according to the second embodiment of the
invention.

Fig. 9 is a block diagram of the construction of a path memory circuit of the LVA detector according to the second embodiment of the invention.

Fig. 10 is a diagram showing the path memory length reducing effect of the LVA detector according to the first embodiment of the invention.

Fig. 11 is a diagram showing the path memory length reducing effect of the LVA detector according to the second embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Some embodiments of a digital magnetic recording/reproducing apparatus of the invention will be described with reference to the accompanying drawings.

Fig. 1 shows the system structure of a digital magnetic recording/reproducing apparatus according to the invention. Referring to Fig. 1, on the recording side, a recording coder 101 converts an input information sequence of 0, 1 of digital data into a high rate code of R=16/17. The recording code, as well known, limits the number of successive 0s to a definite number, thereby preventing the timing extraction and gain control (not shown in Fig. 1) of the reproducing side from being reduced in their performances. The recording coded sequence is then coded for error detection by a CRC coder 102. The CRC can be achieved using a block code produced by adding error detection check bits to the recording

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coded sequence.  Here, the coded sequence is constructed
by blocks of much longer CRC block length (more than
about 100 bits) so that the substantial coding rate after
CRC coding becomes more than 8/9 for high-density

5    recording.  If, for example, CRC check bits of 8 bits are
added to every 8 units each of which is composed of 17
bits after 16/17 code conversion, the CRC block length is
8 units + 8 bits, or 144 bits, and the coding rate
becomes 128/144, or 8/9 as a whole.  Thus, the above CRC

10   block structure is able to detect an arbitrary error of,
for example, up to 2 bits.  Errors can be limited to 2
bits or less by the provision of a precoder 103.  The
precoder 103 converts the CRC coded sequence into a code
using $1/(1 + D^2)$ as a transfer function.  Here, D is the

15   delay operator that provides a delay time equal to the
distance between bits.  The precoder 103 and
reproducing-side postcoders 112 can suppress the decoded
error propagation length after Viterbi detection to a
definite value.  Therefore, the CRC can detect on the

20   reproducing side all error patterns that have been
limited to a definite length by the above means.  The
precoded sequence is supplied through an amplifier 104 to
a record head 105 by which it is recorded as magnetic
information on a magnetic recording medium 106.

25        On the reproducing side, the magnetic information
recorded on the magnetic recording medium 106 is
converted into an analog electric signal by a reproduce

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head 107 and an amplifier 108. This analog signal is sampled at intervals of a bit, thereby being converted into a digital signal by an A/D converter 109. The digital signal is equalized into a partial response

5   channel such as PR4, EPR4, or EEPR4 by a PR equalizing circuit 110. This PR equalization can be easily attained by the well known transversal filter. The output from the PR equalizing circuit 110 contains noise added to a signal level that is determined by the PR channel

10  characteristic. Here, the noise added includes medium noise, mixed noise from the reproduce head, and A/D quantization noise. These noises, when passed through the PR equalizing circuit 110, become colored noises having a correlation. The equalized signal with noise

15  added undergoes MLSE (Maximum Likelihood Sequence Estimation) in an LVA detector 111, which then produces n candidates including the most probable data sequence, or best candidate, in parallel (the arrangement of the LVA detector according to the invention will be described in

20  detail later). The LVA detector according to the invention can be constructed by use of a shorter path memory length than the CRC block length by the technique described in detail later. The n candidates from the LVA detector are reversely converted by the postcoders 112

25  using a transfer function of $1 + D^2$ as opposed to the recording-side precoder 103. Then, the candidates after the postcoding are supplied to CRC error detectors 113,

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where errors are detected.  The candidates produced from the CRC error detectors 113 are fed to a selector circuit 114 together with the associated syndromes.  The selector circuit 114 selects one no-error decided sequence of

5      syndrome 0 from the n input sequences or candidates, and supplies it to a recording decoder 115.  At the same time, an error flag signal of 0 is also produced, and transmitted to a control circuit (not shown) to inform the control circuit that there is no decoding error.

10     This control circuit is a circuit to control the interface between the magnetic recording/reproducing apparatus and a computer.  If none of the candidates has a syndrome of 0, it is decided that a decoding error has occurred, and an error flag signal of 1 is supplied to

15     the control circuit, requesting retransmission.  The recording decoder 115 decodes the sequences, and restores the information sequence.

Figs. 6 and 7 fully show the construction of the LVA detector 111 according to the first embodiment of the

20     invention.  Figs. 6 and 7 respectively show the ACS circuit and the path memory circuit in the LVA detector. Here, there are shown circuit arrangements for producing two candidates (the best and 2nd best sequences).  The construction can be easily expanded to handle three or

25     more candidates.  In addition, although this embodiment illustrates an example of the circuit arrangements using an EPR4 channel, it is possible to similarly construct

circuit arrangements using an arbitrary PR channel, for
example, an EEPR4 channel.

Referring to Fig. 6, the ACS operation is performed
in parallel for every channel state 0, … , 7 (000, … ,
111). Here, the processing for state 0 will be described
as an example. The other states are quite similarly
processed. For the state 0, there are provided four
delay elements 601, which hold state likelihood ratios
S0.1, S0.2, S4.1, S4.2 one sample time (D) before. Here,
Si.j indicates the likelihood ratio of the jth best
sequence (j=1:best, 2:2nd) of state i (i=0, … , 7). At
the present time, when the PR equalized signal is
applied, the squared distances of the differences to an
ideal value (in the case of EPR4ML, 2, 1, 0, −1, −2) are
calculated as branch likelihood ratios BMmn. Here, BMmn
are the branch likelihood ratios of the transition paths
from state m to state n (m, n: 0, … , 7) relative to the
ideal values (see Fig. 3). Here, the circuit for
computing the branch likelihood ratios is not shown. The
likelihood ratios Si.j and the branch likelihood ratios
BMmn are added by adders 602 according to the trellis
diagram shown in Fig. 3. The results of the addition are
fed to a sort circuit 603, which then selects the
maximum, second highest, and third highest likelihood
ratios, and outputs them together with the corresponding
path memory selecting signal P0. P0 is a digital signal
of 6 bits. The 6 bits are necessary because two bits are

utilized to select each of the best, 2nd best, and 3rd best sequences from the four input sequences to the sort circuit. The sort circuit 603 can be easily constructed by a comparator circuit or the like for comparing the input signals. In this embodiment, the sort circuit 603 selects up to the third highest likelihood ratio, which is used, if necessary, as a replacement for the second highest likelihood ratio as will be described later. The sort processing in this embodiment is unlike that in the prior art. It selects the same values if present. If, for example, the four input values are 5.3, 5.3, 3.2, and 1.7, the sort circuit produces at its outputs the values of 5.3, 5.3, and 3.2 as the best, 2nd best, and 3rd best candidates, respectively. In the prior art, since different sequences are always selected, values of 5.3, 3.2, and 1.7 are chosen. The reason why the same values are included in this embodiment is that the LVA is designed to make the path memory length shorter than the CRC block length. If the same values are selected, the associated path memories probably become the same (equal sequences). Therefore, in this case, it is necessary to decide if the same sequence as the best sequence may be treated as the 2nd best sequence, and to make the replacement relative to the 3rd best sequence.

The above processing and the circuit arrangement for this purpose will be described below. The basic idea is that in general when the contents of the $(i-1)$th path

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memory and the ith path memory (i=2, 3, … , n) are
coincident with each other in each state and the absolute
value of the difference between the (i-1)th and (2i-1)th
likelihood ratios is smaller than a decision threshold,

5    the likelihood ratio and the path memory for the ith best
sequence are replaced by those for the (2i-1)th best
sequence.  In this embodiment, since n=2, when the
contents of the first and second path memories coincide
with each other and the absolute value of the difference

10   between the first and third likelihood ratios is smaller
than the threshold, the likelihood ratio and the path
memory for the second best sequence are replaced by those
for the third best sequence.  The detailed construction
of the path memory will be described separately with

15   reference to Fig. 7.  When the contents of the path
memories of the best and 2nd best sequences are
coincident with each other, and when the absolute value
of the difference between the likelihood ratios of the
best and 3rd best sequences is smaller than a decision

20   threshold $\alpha$, the above condition is satisfied.  Thus, the
ACS circuit (Fig. 6) receives a control signal C0=1 from
the path memory circuit (Fig. 7), and supplies it to a
selection circuit 607.  When C0=0, the above condition is
not satisfied.  When C0=1, the selector circuit 607

25   outputs the likelihood ratio of the 3rd best sequence,
and treats it as the likelihood ratio S0.2 of the 2nd
best sequence.  When C0=0, the selector circuit 607

outputs the likelihood ratio of the 2nd best sequence, and treats it as the likelihood ratio S0.2 of the 2nd best sequence (the replacement processing is not performed). The likelihood ratios S0.1 and S0.2 are again stored in the corresponding delay element 601 so as to be ready and waiting for the ACS operation at the next time. Here, the Si.j after sorting is fed back to the corresponding delay element 601 as Si.j as illustrated, but to avoid complexity, no connecting lines are shown.

In the path memory (see Fig. 7), when C0=1, the path memory for the 3rd best sequence and the path memory for the 2nd best sequence are replaced by each other. When C0=0, no replacement is carried out. It is possible to adequately select the 2nd best sequence by the above processing, and as will be described later, the LVA can be achieved using a shorter path memory length than the CRC block length.

For the comparison of likelihood ratios, as shown in Fig. 6, the difference value S0.1-S0.3 is calculated by a subtracter 604, and the absolute value of the difference is obtained by an absolute value circuit (ABS) 605. The absolute value is compared with the threshold $\alpha$ in a comparator circuit 606. When it is smaller than $\alpha$, the control signal A0=1 is supplied to the path memory circuit. If it is not smaller than $\alpha$, the control signal A0=0 is supplied to the path memory circuit. The threshold $\alpha$ is fixed to one-half of MSED. For EPR4ML, $\alpha$

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is 2.  Although the above description is for the
processing in the ACS circuit in the state 0, quite the
same is applied to the other states.

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Fig. 7 shows the arrangement of the path memory
circuit.  The path memory circuit performs register
exchange processing by use of control signals P0, … , P7
(of 6 bits each) produced from the ACS circuit (Fig. 6).
Each of registers 701 has Ri.j written therein.  Here,
Ri.j is the contents of the path memory for the jth best
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(j=1:best, 2:2nd best, 3:3rd best) candidate in the state
i (=0, … , 7).  Data of 0 or 1 is stored over K bits,
where K is the path memory length.  The registers 701 are
shift registers, and are able to output data in parallel.
The control signals P0, … , P7 produced from the ACS
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circuit are supplied to a register exchange circuit 702.
The register exchange circuit 702 exchanges the path
memories to be selected for each of best, 2nd best, and
3rd best sequences on the basis of the control signals
P0, … , P7.  Each control signal is composed of 6 bits
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since two bits are required to select each of the best,
2nd best, and 3rd best sequences (see Fig. 6).  The
output signals after the exchange are supplied as Ri.j'
to comparator circuits 703 and exchange circuits 704.
The details for the state 0 will be described as an
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example.  The other states are processed in the same way.
The output signal R0.1' is fed to the comparator circuit
703 and fed back to the corresponding register 701 (to

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avoid complexity, the connecting lines for feedback to the registers are not shown).  At the same time, the output signal R0.2′ is supplied to the comparator circuit 703 and exchange circuit 704, and the output signal R0.3′

5      is supplied to the exchange circuit 704.  The comparator 703 compares the input signals R0.1′ and R0.2′.  If those signals are equal, the comparator outputs 1.  If they are not equal, the comparator outputs 0.  The output from the comparator 703 is fed to an AND gate 705 together with

10     the control signal A0 from the ACS circuit.  The AND gate 705 outputs the logic product of both signals.  The output C0 from the AND gate 705 is used as the control signal for the exchange circuit 704 and the selector circuit 607 in the ACS circuit.  When C0=1, the exchange

15     circuit 704 performs exchange processing for R0.2=R0.3′, R0.3=R0.2′, and at the same time the selector circuit 607 within the ACS circuit selects S0.3 (the likelihood ratio of the 3rd best sequence).  When C0=0, no exchange processing is performed.  The output from the exchange

20     circuit 704 is R0.2=R0.2′, R0.3=R0.3′, and the output from the selector circuit 607 within the ACS circuit is S0.2 (the likelihood ratio of the 2nd best sequence). The path memories R0.1, R0.2, R0.3 thus finally decided are fed back to the associated registers 701 (to avoid

25     complexity, no connecting lines are shown).

The register 701 after the feedback operates as a shift register so that data 0 or 1 is serially inputted

into the MSB (Most Significant Bit), and so that data 0 or 1 is serially outputted from the LSB (Least Significant Bit) as a decoding result.  In this case, the serially inputted data assumes an EPR4 channel.  The even state (0, 2, 4, 6) is 0, and odd state (1, 3, 5, 7) is 1. The decoded outputs of best and 2nd best sequences of state i (i=0, ... , 7) are $di.1$ and $di.2$, respectively. The finally decoded result of the best sequence is decided by majority from $di.1$ (i=0, ... , 7), or $d0.1$ may be outputted as a typical value.  This is because when the path memory length is sufficiently long, the maximum likelihood decoded results in all states are fundamentally coincident.  For the 2nd best sequence, similarly, the decoded result is decided by majority from $di.2$ (i=0, ... , 7), or $d0.2$ may be outputted as a typical value.

According to this embodiment, the necessary path memory length of the LVA can be reduced to 1/2 the CRC block length (halved as compared with the prior art).

Fig. 10 shows the effect of the path memory length reduction of the LVA.  In Fig. 10, the contents of the path memory for the best and 2nd best sequences are shown when the path memory length is, for example, 1/6 the CRC block length.  If the CRC block length is 144 bits, the path memory length of the LVA is 24 bits.  Here, it is assumed that the S/N ratio in the input to the LVA detector is high enough so that a probability that an

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error event occurs twice or more over the CRC block
length is negligibly small. In addition, it is assumed
that time elapses in the order of memory block number (1,
2, ...) indicated at each memory. As illustrated, an error
5    event occurs in the second memory block, but the decoding
error of the best sequence is covered by the 2nd best
sequence according to the invention. In the prior art,
the best and 2nd best sequences always take different
decoded outputs at each path memory length. Therefore,
10   if the path memory length is shorter than the CRC block
length, the candidates of both best and 2nd best
sequences observed over the CRC block length are detected
as erroneous sequences as illustrated. According to the
invention, the same path memory (correct sequence) except
15   the second memory block is selected for both best and 2nd
best sequences. The likelihood ratios of the best
sequence and the 2nd best sequence are extremely close,
but the absolute value of the likelihood ratio difference
$\Delta M13$ between the best sequence and the 3rd best sequence
20   is larger than the threshold $\alpha$. Thus, both best and 2nd
best sequences can be decided to be sufficiently reliable
as compared with the 3rd best sequence. In the second
memory block, an error event happens, and before
performing the replacement processing according to this
25   embodiment, the same path memory (erroneous sequence) is
selected for both best and 2nd best sequences (since the
likelihood ratios of the best sequence and the 2nd best

sequence are very close to each other). However, here, the absolute value of $\Delta M13$ is smaller than $\alpha$. This suggests that the candidate (correct sequence) considered as being reliable on a likelihood ratio basis is present

5    in the 3rd best sequence at a high probability. Thus, the likelihood ratio and the path memory of the 2nd best sequence are replaced by those of the 3rd best sequence, and the candidate (3rd best sequence) different from the best sequence is selected as the 2nd best sequence. The

10   above replacement processing makes it possible that a correct decoded sequence is included in either one of the best and 2nd best sequences of even the second memory block. As described above, only the true error event can be corrected and correct decoded outputs can be produced

15   by use of the 2nd best sequence over the CRC block length.

Thus, according to this embodiment, when the path memories of the best and 2nd best sequences are equal, it is decided if the likelihood ratio of the 3rd best

20   sequence is close to that of the best sequence by comparing the absolute value of the difference between them with the threshold $\alpha$. If it is close, the 3rd best sequence is selected as the 2nd best sequence. If it is not close, the 2nd best sequence is selected as it is.

25   This means that even when the best sequence and the 2nd best sequence are equal, both candidates can be decided to be reliable as long as the likelihood ratio difference

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relative to the 3rd best sequence is sufficiently large. In other words, in this embodiment, when the S/N ratio of the reproduced signal is high enough, the best and 2nd best sequences are fundamentally equal. Also, only when

5    the reliability of the 3rd best sequence is high on a probability basis (the absolute value of the likelihood ratio difference relative to the best sequence is smaller than the threshold $\alpha$), the 3rd best sequence (different from the best sequence in most cases) is selected as the

10   2nd best sequence, thus covering the decoding error. In the conventional system, the starting state and the ending state in the trellis diagram were periodically fixed to one state, and the likelihood ratios of all candidates in the starting state were initialized to be

15   the likelihood ratio of the best sequence so that a different candidate could always be obtained at each path memory length. Therefore, the possible coding rate was low, and the path memory length could not be made shorter than the CRC block length. According to the invention,

20   since a different sequence is not necessarily selected as a candidate at each path memory length, all error phenomenon of any CRC (see Fig. 5 at (b) and Fig. 10) can be prevented, and the path memory length can be made shorter than the CRC block length. In addition, since

25   the likelihood ratios of candidates are equivalently initialized by the likelihood ratio replacement described above, there is no need to periodically fix the starting

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and ending states to one state in the trellis diagram and
no need to initialize the likelihood ratios of all
candidates in the starting state, thereby enabling a high
coding rate of 8/9 or above to be attained.   The

5    likelihood ratio initialization (the above replacement
processing) according to the invention resets by the
replacement the likelihood ratio difference between the
best and 2nd best sequences, which difference is narrowed
with time, thereby making it possible to objectively

10   select candidates so that the same sequence as the best
sequence cannot be unilaterally chosen as the 2nd best
sequence.   According to the invention, the likelihood
ratio initialization is performed not periodically as in
the prior art, but it is performed only as required,

15   thereby realizing the high-rate coding and necessary path
memory length reduction.

     Figs. 8 and 9 show detailed constructions of the LVA
detector according to the second embodiment of the
invention.   Figs. 8 and 9 respectively show block

20   diagrams of the ACS circuit and the path memory circuit
in the LVA detector.   Here, circuit arrangements are
shown which produce two candidates (the best and 2nd best
sequences).   The circuit arrangements can be easily
expanded to produce three or more candidates.   In

25   addition, although this embodiment is an example of using
an EPR4 channel, it can be similarly modified for the

arrangements using an arbitrary PR channel, for example, an EEPR4 channel.

Referring to Fig. 8, the ACS operation is performed for channel states 0, ... , 7 (000, ... , 111, respectively) in parallel. Here, the processing for state 0 will be described as an example. The processing for other states can be performed in quite the same way. In state 0, four delay elements 801 are provided to store state likelihood ratios S0.1, S0.2, S4.1, S4.2 one sample time (D) before. Here, Si.j is the likelihood ratio of the jth best candidate (j=1:best, 2:2nd best) in the state i (i=0, ... , 7). At the present time, when a PR equalizing signal is applied, the squared distance of the difference relative to the ideal value (2, 1, 0, -1, -2 for EPR4ML) is calculated as a branch likelihood ratio BMmn. Here, BMmn is the branch likelihood ratio to a PR equalizing ideal signal (see Fig. 3) of the transition path from state m to state n (m, n: 0, ... , 7). Also, the circuit for computing the branch likelihood ratio is not shown. The likelihood ratio Si.j and the branch likelihood ratio BMmn are added by adders 802 according to the trellis diagram shown in Fig. 3. The added results are fed to a sort circuit 803, which then selects the maximum likelihood ratio S0.1 and the second best likelihood ratio S0.2, and outputs them together with the corresponding path memory selecting signal P0. Here, P0 is a digital signal of 4 bits, because two bits are

necessary for each of the best and 2nd best sequences to be selected. The adder 802 adds the output S0.1 and a constant difference value $\Delta S$ to produce a corrected value S0.1' as an output, which is then supplied to a selection circuit 804 together with S0.2. The difference value $\Delta S$ is fixed to the MSED value. In the case of EPR4ML, $\Delta S$ is equal to 4. The sort circuit 803 can be easily constructed by a comparator for comparing the magnitudes of the inputs. The sort processing in this embodiment is unlike that in the prior art. In other words, even if the same values are present, they are selected. If, for example, the four input values are 5.3, 5.3, 3.2, and 1.7, the sort circuit produces 5.3 and 5.3 as the best and 2nd best values at its outputs, respectively. In the prior art, since different sequences are always selected, the sort circuit chooses 5.3 and 3.2. In this embodiment, the same values are selected in order to realize the LVA by use of a shorter path memory length than the CRC block length. If the same values are selected, the corresponding path memories probably become the same (the same sequence). Thus, in this embodiment, when the path memory for the best sequence is the same as that for the 2nd best sequence, the likelihood ratio of the best sequence is corrected and the corrected likelihood ratio is initialized to be the likelihood ratio of the 2nd best sequence. The likelihood ratio initialization in this invention is performed so that the

likelihood ratio difference between the best and 2nd best
sequences, which difference is narrowed with time, is
again established by the initialization processing, and
so that the candidates are objectively selected without

5   unilaterally choosing a sequence equal to the best
sequence as the 2nd best sequence. According to the
invention, the likelihood ratio initialization is
performed only if necessary, unlike in the conventional
system in which it was performed periodically. Thus, the

10   system according to the invention can attain the
high-rate coding and necessary path memory length
reduction.

     The initialization processing and the circuit
arrangement for performing this processing will be

15   described below. The basic idea is that in general when
the contents of the $(i-1)$th path memory coincide with
those of the ith $(i=2, 3, \ldots, n)$ path memory in each
state, the likelihood ratio of the $(i-1)$th best sequence
is added with a constant difference value $\Delta S$, and the sum

20   is initialized to be the likelihood ratio for the ith
best sequence. In this embodiment, since $n=2$, when the
contents of the first and second path memories are
coincident in each condition, the likelihood ratio of the
first best sequence is added with the constant difference

25   value $\Delta S$, and the sum is initialized to be the likelihood
ratio for the second best sequence. The detailed

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construction of the path memory will be separately
described with reference to Fig. 9.

When the contents of the path memory for the best
sequence are coincident with those for the 2nd best
sequence, the above conditions are satisfied, and thus
the ACS circuit receives the control signal $B0=1$ from the
path memory circuit, and supplies it to the selection
circuit. When $B0=0$, the above conditions are not
satisfied. When $B0=1$, the selector circuit outputs the
corrected likelihood ratio $S0.1'$ of the best sequence as
the likelihood ratio $S0.2$ of the 2nd best sequence. When
$B0=0$, the selection circuit outputs the likelihood ratio
$S0.2$ of the 2nd best sequence as the likelihood ratio
$S0.2$ of the 2nd best sequence. The likelihood ratios
$S0.1$ and $S0.2$ are again stored in the corresponding delay
elements 801 to be ready and wait for the ACS operation
at the next time. The $Si.j$ after sorting is fed back to
the corresponding delay element 801 as $Si.j$ as
illustrated, but the connecting lines are not shown to
avoid complexity.

Fig. 9 shows the arrangement of the path memory
circuit. In the path memory circuit, the control signals
$P0, \ldots, P7$ (4 bits each) produced from the ACS circuit
(Fig. 8) are used to perform register exchange
processing. Each of registers 901 has $Ri.j$ written
therein. Here, $Ri.j$ is the contents of the path memory
associated with the jth best (j=1:best, 2:2nd best)

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candidate in state i (=0, … , 7).  Data 0 or 1 are stored
over K bits.  Here, K is the path memory length.  The
registers 901 are shift registers each capable of
outputting data in parallel.  The control signals P0, … ,

5    P7 produced from the ACS circuit are supplied to a
register exchange circuit 902.  The register exchange
circuit 902 is responsive to the control signals P0, … ,
P7 to exchange the path memories to be selected for each
of the best and 2nd best sequences.  Each control signal

10   is composed of 4 bits because two bits are required to
select each of the best and 2nd best sequences (see Fig.
8).  The outputs after exchange are supplied as Ri.j' to
comparator circuits 903, and are also fed back to the
corresponding registers 901 (the feedback connection

15   lines are not shown to avoid complexity).  The case of
state 0 will be described in detail as an example.  The
other states can be similarly processed.  The outputs
R0.1' and R0.2' are supplied to the comparator circuit
903, and at the same time are fed back to the

20   corresponding registers 901.  The comparator circuit 903
compares the input signals R0.1' and R0.2'.  If both
input signals are equal, 1 is output from the comparator
to the ACS circuit as the control signal B0.  If both
input signals are not equal, 0 is similarly output as B0.

25   When B0=1, the selection circuit 804 in the ACS circuit
outputs S0.1' (the corrected value of S0.1).  When B0=0,

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the selection circuit 804 in the ACS circuit outputs S0.2
(the likelihood ratio of the 2nd best sequence).

The register after feedback operates as a shift
register so that data 0 or 1 is serially inputted into
5   the MSB (Most Significant Bit), and so that data 0 or 1
is serially outputted as a decoding result from the LSB
(Least Significant Bit).  Here, the serially inputted
data assumes an EPR4 channel.  The even state (0, 2, 4,
6) is 0, and the odd state (1, 3, 5, 7) is 1.  The
10  decoded outputs for the best and 2nd best sequences in
state i (i=0, ... , 7) are di.1 and di.2, respectively.
The final decoded result for the best sequence is decided
as di.1 (i=0, ... , 7) by majority, or d0.1 may be
outputted as a typical value, because when the path
15  memory length is long enough, the maximum likelihood
decoded result in any state is fundamentally the same.
The final decoded result for the 2nd best sequence is
similarly decided as di.2 (i=0, ... , 7) by majority, or
d0.2 may be outputted as a typical value.

20  According to this embodiment, the necessary path
memory length of the LVA can be reduced to 1/2 the CRC
block length (halved as compared with the prior art).
Therefore, this embodiment is effective when the CRC
block length is relatively short.

25  Fig. 11 shows the effect of the path memory length
reduction of the LVA according to this embodiment.  The
contents of the path memories for the best and 2nd best

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sequences are shown in the case where the path memory
length is 1/2 the CRC block length.  If the CRC block
length is 50 bits, the path bit memory length of the LVA
is 25 bits.  Here, it is assumed that the S/N ratio in
5    the input to the LVA detector is large enough to consider
a probability that an error event occurs twice or more
over the CRC block length to be negligibly small.  In
addition, it is assumed that time elapses in the order of
memory block number (1, 2, ...) indicated at each path
10   memory.  As illustrated, an error event occurs in the
first memory block, and the present invention covers the
decoded error of the best sequence by use of the 2nd best
sequence.  In the prior art, different decoded outputs
are always produced in the best and 2nd best sequences at
15   each path memory length.  Therefore, when the path memory
length is shorter than the CRC block length, both best
and 2nd candidates observed over the CRC block length
will be detected as erroneous sequences.  According to
the invention, both best and 2nd best sequences select
20   the same path memory (correct sequence) in the second
memory block.  Even when the likelihood ratios of the
best sequence and 2nd best sequence are equal or very
close, they are selected in the sort processing.  In this
invention, however, the likelihood ratio of the 2nd best
25   sequence is, at this time, initialized by the
initialization processing.  Thus, in the third memory
block (not shown), the best and 2nd best sequences select

different path memories.  By the above-described
initialization processing, it is possible to ensure that
a correct decoded sequence is included in either one of
the best and 2nd best sequences.  Thus, over the CRC

5   block length, only true error events can be corrected,
and thus correct decoded outputs can be obtained in the
2nd best sequence.

        As described above, according to this embodiment,
when the path memories of the best and 2nd best sequences

10  are equal, the likelihood ratio of the best sequence is
corrected and initialized to be the likelihood ratio of
the 2nd best sequence.  In the prior art, the starting
state and the ending state in the trellis diagram were
periodically fixed to one state, and the likelihood

15  ratios of all candidates in the starting state were
initialized to be the likelihood ratio of the best
sequence.  Thus, different candidates were always
obtained at each path memory length.  Accordingly, the
possible coding rate was low, and the path memory length

20  could not be made shorter than the CRC block length.
According to the invention, since a different sequence is
not necessarily proposed, or selected as a candidate at
each path memory length, the phenomenon that the CRC
becomes erroneous at all times (see Fig. 5 at (b) and

25  Fig. 11) can be prevented, and the path memory length can
be made shorter than the CRC block length.  In addition,
since the likelihood ratios of the candidates are

equivalently initialized by the likelihood ratio
initialization processing as described above, there is no
need to periodically fix the starting state and the
ending state in the trellis diagram to one state and no
5   need to initialize the likelihood ratios of all
candidates in the starting state.  Thus, a higher coding
rate than in the prior art can be attained.  The
likelihood ratio initialization according to the
invention is to again set by the correction the
10  likelihood ratio difference between the best and 2nd best
sequences, which difference is narrowed with time, and to
objectively select the candidates so as not to
unilaterally select a sequence equal to the best sequence
as the 2nd best sequence.  According to the invention,
15  since the likelihood ratio initialization is performed
only if necessary, not periodically as in the
conventional system, higher rate coding and the reduction
of necessary path memory length can be achieved.

   The embodiments of the invention as described above
20  are easily expandable even when three or more candidates
are used in the LVA.  In addition, these embodiments can
be applied to an arbitrary channel, for example, an EEPR4
channel.

   Thus, according to the invention, the necessary path
25  memory length of the LVA detector can be reduced to less
than half the CRC block length, and the LVA structure can
be made simpler than in the prior art.  In addition,

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since the likelihood ratio difference between candidates can be initialized without periodically fixing the starting and ending states in the trellis diagram to one state, the coding rate can be increased to a higher value of 8/9 or more.

The present invention can be easily expanded so that three or more candidates can be used in the LVA, and can also be applied to an arbitrary PR channel, for example, an EEPR4 channel. Therefore, the invention can provide a digital magnetic recording/reproducing apparatus having a simple construction and being capable of high-density recording.